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Uniformity and process stability of the slot-die coated PTB7:$PC_{71}BM$ organic photovoltaic improved by solvent additives

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HIGHLIGHTS

- Slot-die coating of organic solar cell and module with improved uniformity and process stability.
- Add solvent additives in active layer to control the uniformity of slot-die films.
- Tune the substrate temperature to control the BHJ film morphology.
- Large-area devices and module with low power conversion efficiency loss.

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ABSTRACT

In this study, the organic photovoltaics (OPVs) with bulk heterojunction (BHJ) structure based on the active layer of PTB7:$PC_{71}BM$ and fabricated by sheet-to-sheet slot-die coating process are prepared to evaluate the uniformity and process stability of the active layer on cell performance. Various solvent additives are mixed in the host solvent o-xylene for improving the performance of low band-gap based polymer system. The solvent additives as recipe will influence the drying rate as well as the nano-BHJ morphology of the active layer. The residual solvent left in the dried film plays an important role in determining the uniformity and performance of organic photovoltaics. Thus, we comparatively investigate the correlation between recipes using solvent additives and different substrate temperature on sheet-to-sheet (S2S) system. OPV with active areas of range from 1 × 0.3, 1 × 1, 1 × 2 to 1 × 4 cm^2 are fabricated to verify the performance of the scale-up devices. The temperature-independent feature of substrate is demonstrated for the recipe of 1.5 vol% 1,8-diiodooctane (DIO) plus 1.5 vol% 1-chloronaphthalene (CN). Less performance loss of 2.7% is shown at the active area of 1 × 4 cm^2 compared to that of 16.1% for the recipe of 3 vol% DIO. The results will facilitate the scalable commercialization due to several merits of broad process window of S2S slot-die coating process, high film uniformity and high reproducibility between batches, and high power conversion efficiency.

1. Introduction

Organic photovoltaics (OPVs) are considered to be a clean and renewable energy technology, and have attracted tremendous attention over the past decades due to several advantages of light weight, mechanical flexibility, low cost, low energy payback time, ease of fabrication, and tunable color appearance [1–3]. Besides, OPVs can readily use solution processing for large area production and thus increase the competitiveness of the commercialization. OPVs can be designed with a high freedom, facilitating some applications like Internet of things (IoT), building-integrated photovoltaics (BIPV), wearable electronics, portable charger, and be integrated with any shape like human body [4,5], etc. However, the relatively low power conversion efficiency (PCE) compared to other kinds of solar PVs is always challenged. Because of the exploitation of novel low band-gap conducting polymer materials, non-fullerene acceptors (NFAs), and well-developed bulk heterojunction

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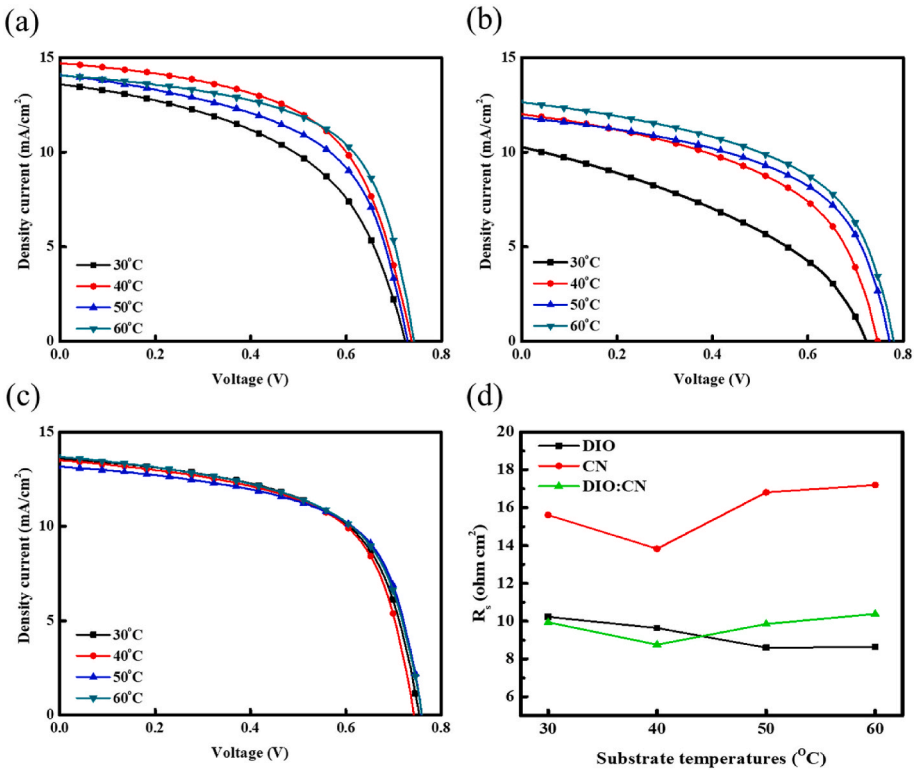

Fig. 1. J-V curves of S2S slot-die coated OPV devices based on various solvent additives at different substrate temperatures: (a) 3 vol% DIO, (b) 3 vol% CN, and (c) 1.5 vol% DIO: 1.5 vol% CN. (d) Sheet resistance (R_s) statistics for each active layer solution formulation at different substrate temperatures. The device area is 0.3 (1 × 0.3) cm^2. All the devices are fabricated in the same batch.

(BHJ) structure, the PCE of OPV devices is continuously increasing, the champion record over 18% is achieved up-to-date [6].

Solution processing have been widely used commercially promising fabrication methods since they can easily and rapidly produce large-area functional layers under ambient condition, avoiding huge investment of expensive vacuum and deposition system. Several printing techniques, including slot-die coating [7–13], spray coating [14–17], inkjet printing [18–20], screen printing [8,21,22], have been verified by various layers in OPV devices and demonstrate the up-scaling feasibility in large-area, and high throughput process. Slot-die coating, one of the most potential printing methods for commercialization among the non-contact wet processing technique, can be utilized to deposit homogeneous films with high uniformity and reproducibility. In addition, slot-die coating method exhibits a high compatibility of integration with roll-to-roll (R2R) and sheet-to-sheet (S2S) process and thus reduces the gap from laboratory to mass-production fabrication.

The active layer of devices consisting of conducting polymers as electron donor and fullerene derivatives as electron acceptor has a bi-continuous interpenetrating network morphology, called BHJ structure, for facilitating the charge generation and transportation, and improving the PCE of OPVs. Moreover, the development of low band gap conducting polymer enhances the PCE dramatically due to a broad absorption spectrum. Among these devices based on low band gap polymer, OPVs with a blend of poly[[4,8-bis[(2-ethylhexyl)oxy] benzo [1,2-b:4,5-b']dithiophene-2,6-diyl] [3-fluoro-2-[(2-ethylhexyl) carbonyl] thieno [3,4-b] thiophenediyl]] (PTB7) and [6,6]-Phenyl C_{71} butyric acid methyl ester ($PC_{71}BM$), are comprehensively discussed in literatures [23–28]. In this system, solvent additives are usually mixed with the PTB7:$PC_{71}BM$ solution to achieve good polymer crystallinity and BHJ nanostructure of the active layer for improving PCE of OPVs. The most commonly used solvent additives are 1-chloronaphthalene (CN) and 1, 8-Diiodooctane (DIO) due to their high boiling point [29]. However, the residual additives in the dried film of the active layer would have a negative impact to OPVs, not only lowering the PCE of the devices, but also increasing the instability of the film quality [30]. The effect of additives on the formation of film BHJ morphology and PCE of the S2S slot-die coated OPVs is under-investigated in the literature compared to the extensive studies on the spin-coated OPVs. The mechanism formation of BHJ layer by S2S slot-die coating is different from that by spin-coating. In this work, we improve the stability of manufacturing process and performance of PTB7:$PC_{71}BM$ based OPVs by tuning the solvent additives. The active layers of PTB7:$PC_{71}BM$ were prepared by S2S slot-die coating technique. Organic additives were varied to prepare the organic active layer with combination of controlling different substrate temperatures. The performance of the S2S slot-die coated OPVs based on different additives and substrate temperatures were comparatively discussed. Our results show a PCE improvement of S2S slot-die coated OPVs with single additive (3 vol% DIO or 3 vol% CN) while the substrate temperature increasing from 30 °C to 60 °C. Moreover, the variation of PCE with single additive under the influence of different batches also converges with increasing the substrate temperature. It is noted that the PCEs of OPVs with mixture of two additives (1.5 vol% CN and 1.5 vol% DIO) keep stable as the substrate temperature ranges from 30 °C to 60 °C. The substrate-temperature-independent phenomenon implies that the broadened process window facilitates the coating process control in the production stage, and reduces the energy payback time (EPBT) of the OPVs. Also, the uniformity of active layers is modified. The PCEs of devices with mixture of two additives are better than those with single solvent additive regardless of large-area devices or modules.

2. Experimentals

Materials. The ITO-coated glass substrate was purchased from Optical Filters Ltd. (EMI-ito 15, surface resistance of 13 Ω/square). Zinc acetate and aluminum acetate were obtained from Alfa Aesar and

Table 1
Photovoltaic characteristics of S2S slot-die coated devices based on various additives and substrate temperatures. The device area is 0.3 (1 × 0.3) cm^2, and the data are averaged over 20 devices. All the devices are fabricated in the same batch.

Additive	Temperature (°C)	J_{SC} (mA/cm^2)	V_{oc} (V)	FF (%)	PCE (%)	PCE_{max} (%)
DIO	30	13.62 ± 0.14	0.73 ± 0.01	50.93 ± 1.65	4.95 ± 0.27	5.27
	40	14.70 ± 0.05	0.74 ± 0.00	58.13 ± 1.53	6.30 ± 0.13	6.43
	50	13.86 ± 0.48	0.74 ± 0.00	57.18 ± 1.59	5.84 ± 0.26	6.22
	60	13.93 ± 0.35	0.74 ± 0.01	59.93 ± 0.38	6.16 ± 0.24	6.41
CN	30	10.38 ± 0.32	0.73 ± 0.00	40.90 ± 1.68	3.08 ± 0.21	3.26
	40	12.03 ± 0.11	0.74 ± 0.01	50.23 ± 1.18	4.50 ± 0.18	4.73
	50	11.80 ± 0.28	0.77 ± 0.01	54.00 ± 0.27	4.90 ± 0.18	5.13
	60	12.63 ± 0.08	0.78 ± 0.01	53.35 ± 1.30	5.24 ± 0.07	5.29
CN:DIO	30	13.50 ± 0.06	0.75 ± 0.01	58.60 ± 1.44	5.92 ± 0.25	6.13
	40	13.54 ± 0.37	0.74 ± 0.01	59.58 ± 1.47	6.00 ± 0.21	6.28
	50	13.11 ± 0.27	0.75 ± 0.01	60.73 ± 0.85	6.00 ± 0.24	6.23
	60	13.69 ± 0.17	0.76 ± 0.01	58.92 ± 0.29	6.11 ± 0.11	6.23

Aldrich, respectively. The surfactant Zonyl FS-300 was purchased from Fluka. Polyethylenimine ethoxylated (PEIE) received from Aldrich was diluted in 2-methoxyethanol into 0.4 wt% of solution. We prepared the precursor of aluminum doped zinc oxide (AZO) solution by dissolving zinc acetate (1 g), aluminum acetate (0.015 g) and Zonyl FS-300 (0.06 g) in 10 g of deionized water (DIW). The as-prepared AZO precursor was filtered through a 0.45 μm filter, and then diluted with DIW by the volume ratio of 1:1. After that, the AZO precursor was mixed with 20 vol % of PEIE to form a hybrid solution of AZO:$PEIE_{20}$ (for preparing the electron transporting layer, ETL). PTB7 and $PC_{71}BM$ were provided by 1-Materials and Rieke Metals, respectively. We prepared the active layer solution by dissolving 7 mg of PTB7 and 10.5 mg $PC_{71}BM$ in 1 ml o-xylene solution followed by addition of different volume concentration of solvent additives.

S2S slot-die coating process for OPV fabrication. We slot-die coated the ETL and photoactive layer by using Coatema S2S system (Coatema easycoater, Germany). The widths of slot-die coater and ITO-glass substrate are 10 and 7 cm, respectively. The coating speeds used for ETL and active layer are 0.5 and 2 m/min, respectively. The solution output rates for coating the ETL and active layer are 0.22 and 1.5 ml/min, respectively, using a mask of 100 μm thickness. Prior to the ETL deposition, the ITO-coated glass substrate was ultrasonically cleaned in a series of organic solvents (methanol, acetone and isopropanol), and then treated with O_2 plasma for 3 min. The substrate temperature for ETL deposition is set at 40 °C, and then dried the deposited ETL at 150 °C for 10 min in the ambient oven. For the photovoltaic devices fabrication, the different substrate temperatures as coating parameter are set at the range from 30 °C to 60 °C with an interval of 10 °C for drying the deposited wet active layer without further thermal annealing. The dried thicknesses of ETL and active layer are about 40 and 85 nm, respectively. We thermally evaporated hole transport layer (HTL) of MoO_3 and silver electrode on the active layer in a separate thermal evaporator. The thicknesses of MoO_3 and silver were 5 nm and 100 nm, respectively. The structure of the devices is PET/ITO/ETL/PTB7:$PC_{71}BM$/MoO_3/Ag. The device area is defined by the metal electrode with the different areas. It is noteworthy to mention that all the S2S coating processes were conducted in air, and all the devices are not encapsulated.

Performance measurement and structural characterization. Current density–voltage curves were measured by using a solar

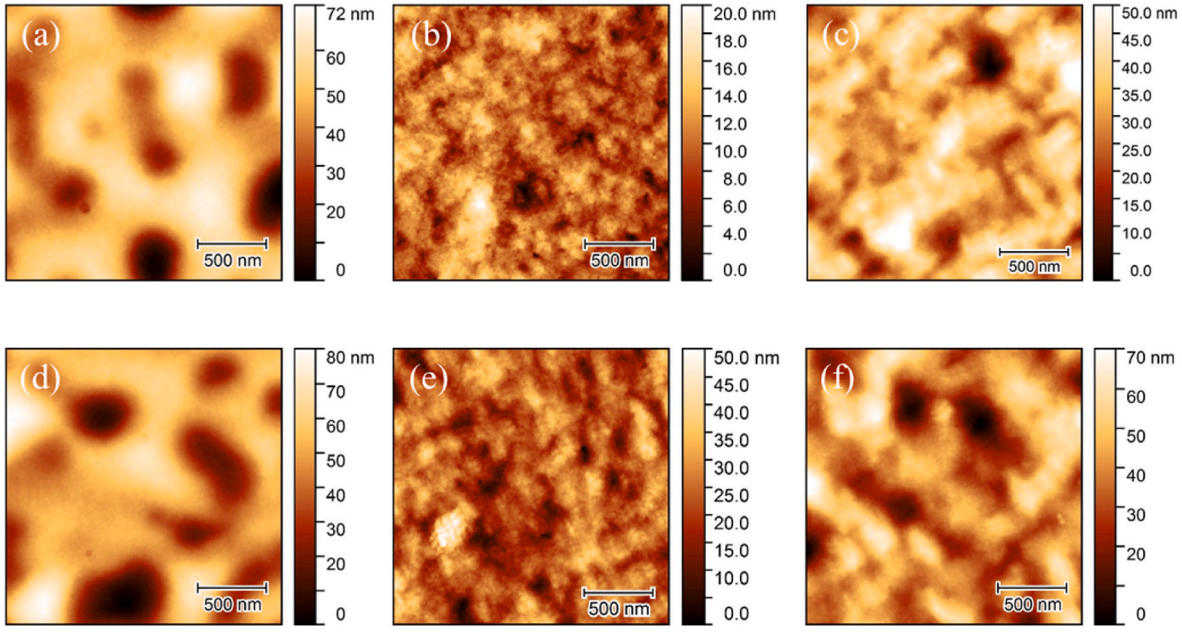

Fig. 2. Atomic force microscopy images of the S2S slot-die coated PTB7:$PC_{71}BM$ films prepared with various additives and at different processing temperatures of 30 °C (a–c) and 50 °C (d–f). These films are with (a, d) 3 vol% CN, (b, e) 3 vol% DIO and (c,f) 1.5 vol% DIO:1.5 vol% CN.

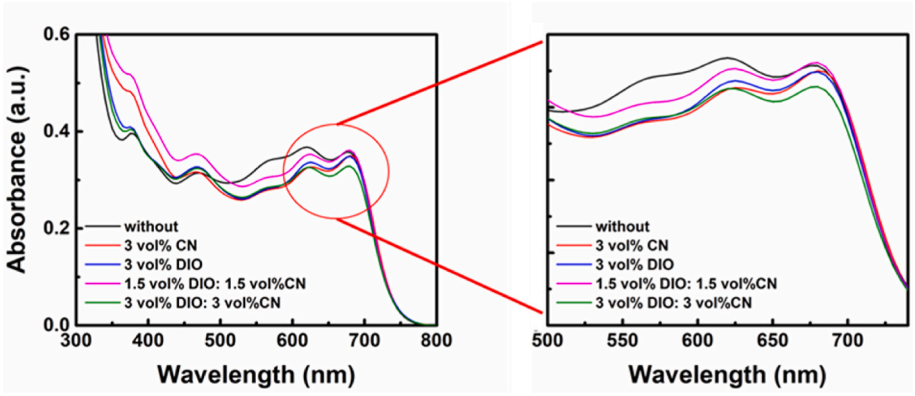

Fig. 3. UV–vis absorption spectra of active layers with various solvent additive systems.

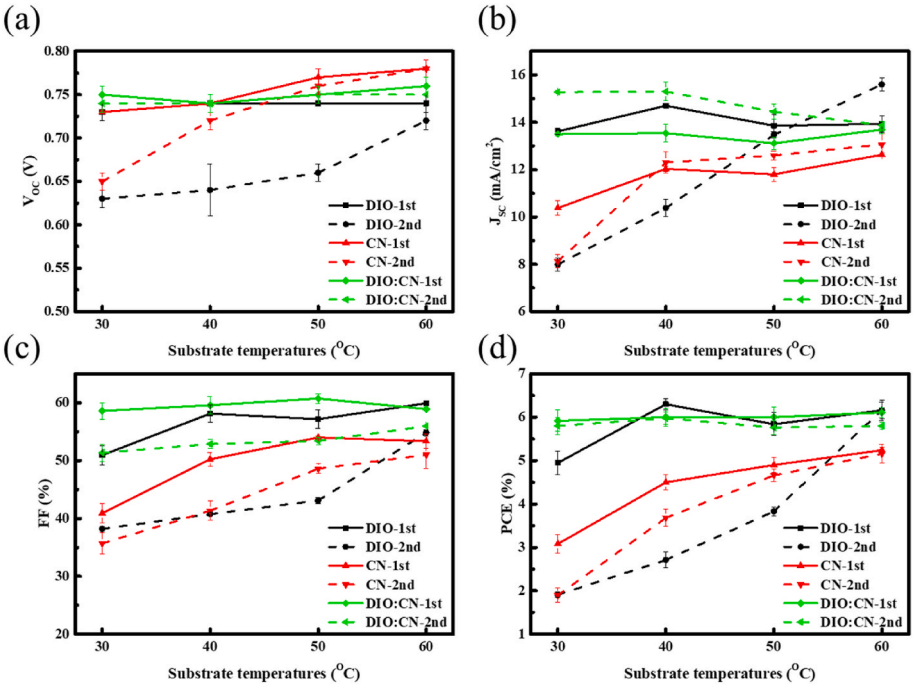

Fig. 4. Comparison of photovoltaic parameters variation of different batches of S2S slot-die coated OPV devices based on various solvent additives at different substrate temperatures. The device area is 0.3 (1 × 0.3) cm^2, and the data are averaged over 20 devices. All the devices are fabricated in the same batch.

simulator (Enli Tech SS-X100R) under A.M. 1.5 illumination (100 mW/cm^2) and ambient condition. The thicknesses of films were measured by a profilometer (Alpha Step D-100, KLA Tencor). Surface roughness and morphology of the blend films were analyzed by atomic force microscopy (Park XE70). The UV–vis absorption of the PTB7:$PC_{71}BM$ films were obtained using a UV–vis spectrometer (Jasco V670). The series resistance (R_s) of OPVs were evaluated based on the measured J-V curves.

3. Results and discussion

According to previous reports [24,27], addition of additive to host solvent increases drying time (or crystallization) of spin-coated active layer as well as the PCE of OPV. However, the residual solvent additive in dried active layer may induce the instable performance of slot-die coated OPV at different batches. In our previous work [31], a different feature was found that the PCE of OPVs can be determined by oven temperature in R2R slot-die coated process. A high drying temperature of 110 °C associated with the fast drying time was proved to be an optimal condition. Since the PCE of the slot-die coated OPV is influenced by the drying temperature, the active layers fabricated at various substrate temperatures in S2S process should be clarified regarding different addition of solvent additives. The different substrate temperatures as coating parameter are set at the range from 30 °C to 60 °C with an interval of 10 °C for drying the deposited wet active layer. The drying rate was increased with the increasing substrate temperature. Firstly, 3 vol% of DIO additive and 3 vol% of CN additive were added respectively in the host solvent of o-xylene to study the influence on PCE at different substrate temperatures. Then, the two additives with equal amount were mixed to form the DIO:CN additive of 1.5 vol% DIO and 1.5 vol% CN. Fig. 1 shows the current density-voltage (J-V) curves and R_s variation of S2S slot-die coated OPV devices based on various solvent additives at different substrate temperatures. Table 1 summarizes the averaged device performance parameters. The PCE of devices based on DIO additive was low at substrate temperature of 30 °C, but achieved a high and stable performance at substrate temperatures range from 40 °C to 60 °C. The best average performance of devices with DIO was obtained at the substrate temperature of 40 °C, with an open-circuit voltage (V_{oc}) of

Table 2
Photovoltaic characteristics of S2S slot-die coated devices in second batch based on various additives and substrate temperatures. The device area is 0.3 (1 × 0.3) cm^2, and the data are averaged over 20 devices. All the devices are fabricated in the same batch.

Additive	Temperature (°C)	J_{SC}(mA/cm^2)	V_{oc}(V)	FF(%)	PCE (%)	PCE_{max}(%)
DIO	30	7.99 ± 0.29	0.63 ± 0.01	38.20 ± 0.42	1.91 ± 0.07	1.97
	40	10.38 ± 0.36	0.64 ± 0.03	40.75 ± 0.29	2.71 ± 0.18	2.87
	50	13.47 ± 0.13	0.66 ± 0.01	43.10 ± 0.56	3.83 ± 0.10	3.94
	60	15.60 ± 0.29	0.72 ± 0.01	54.83 ± 0.55	6.16 ± 0.19	6.35
CN	30	8.13 ± 0.27	0.65 ± 0.01	35.70 ± 1.84	1.90 ± 0.17	2.06
	40	12.30 ± 0.45	0.72 ± 0.01	41.33 ± 1.66	3.68 ± 0.20	3.94
	50	12.60 ± 0.19	0.76 ± 0.01	48.60 ± 0.85	4.66 ± 0.14	4.8
	60	13.06 ± 0.45	0.78 ± 0.01	51.03 ± 2.38	5.16 ± 0.22	5.35
DIO:CN	30	15.28 ± 0.06	0.74 ± 0.01	51.35 ± 1.44	5.80 ± 0.20	5.96
	40	15.30 ± 0.39	0.74 ± 0.01	52.88 ± 0.73	5.98 ± 0.14	6.17
	50	14.45 ± 0.33	0.75 ± 0.01	53.40 ± 0.65	5.76 ± 0.16	5.95
	60	13.87 ± 0.18	0.75 ± 0.00	55.95 ± 0.13	5.80 ± 0.08	5.87

0.74 V, a J_{sc} of 14.70 mA/cm^2, a FF of 58.13%, and a PCE of 6.30%. The PCE of devices with DIO additive showed good performance at the substrate temperature above 40 °C, and it might be attributed to the formation of better nano-structured morphology of PTB7:$PC_{71}BM$ by the addition of DIO additive, which enhances the charge carrier separation and transport properties in the active layer. The PCE of devices prepared with CN additives increased with increasing substrate temperatures, and the best average performance of devices with addition of CN was obtained at the substrate temperature of 60 °C, with a V_{oc} of 0.78 V, a J_{sc} of 12.63 mA/cm^2, a FF of 53.35%, and a PCE of 5.24%. The relative low J_{sc} and FF compared to those devices with addition of DIO can attribute to poor phase separation of active layer that reduces the interface between acceptor and donor and thus decreases the percolation pathways for transporting charge carriers to the relative electrode [24,32,33]. Furthermore, we mixed those two additives into a new solvent additive; the PCE of devices prepared with DIO:CN additive remained unchanged at the substrate temperature range from 30 °C to 60 °C, and a high and stable performance was achieved. The best average performance of devices with addition of DIO:CN additive was obtained at the substrate temperature of 60 °C, with a V_{oc} of 0.76 V, a J_{sc} of 13.69 mA/cm^2, a FF of 58.95%, and a PCE of 6.11%. The substrate temperature-independent feature of the devices based on DIO:CN solvent additive leads to a broader processing window for S2S slot-die coated devices. Moreover, the low operating substrate temperature could reduce the energy consumption as well as the energy payback time.

Fig. 2 shows the surface morphologies of the active layer with different solvent additives under 30 °C and 50 °C. The surface morphology of the films with 3% CN, 3% DIO and 1.5% CN:1.5% DIO under 30 °C are shown in Fig. 2a, b and 2c, respectively. Compared with the active layer containing 3% DIO, the active layer containing 3% CN exhibited obvious phase separation and high roughness (10.15 nm). The result indicates that the active layer with smooth surface and good phase separation (active layer with 3% DIO) can have better PCE. In addition, the PCE of devices with 3% DIO increased further as the processing temperature raised, indicating the active layer exhibited improved phase separation and surface roughness (6.55 nm). The well phase-separated BHJ structure and surface roughness imply that the charge transport behavior and interfacial contact between active layer and top electrode are significantly enhanced. However, in comparison to the 3% DIO active layer with 3% DIO fabricated at 50 °C, the active layer with DIO:CN additive exhibits a comparable phase separation and surface roughness (7.9 nm) at a processing temperature of 30 °C. Therefore, the devices fabricated from the active layer with DIO:CN additive already exhibit excellent PCE at a processing temperature of 30 °C. The phase separation of the films with DIO:CN did not change significantly even with elevated processing temperature. This result is consistent with the substrate temperature-independent feature of the devices based on DIO:CN.

We observed the crystallization behavior and nanostructure of the active layer with different additives by UV–Vis absorption spectrum. The absorption regions of 300–500 nm and 600–750 nm in Fig. 3 are mainly from $PC_{71}BM$ and PTB7 absorption, respectively. The intensity of the absorption peaks represents the crystallinity degree of these molecules. These results indicate that the solvent additives do not have much effect on the crystallinity of PTB7, and over addition would reduce the crystallinity. However, the solvent additives obviously influence molecular arrangement of PCBM, good PCBM arrangement would increase the absorption. Our result implies that the devices with mixing solvent additives of 1.5%DIO:1.5%CN exhibits the best nanostructure of the active layer.

As mentioned above, the PCE of the devices were affected by the residual additive in the active layer, thus the OPV devices might exhibit quite different performance batch by batch under the same processing parameters. Therefore, we did a second batch of OPVs, and the photovoltaic parameters varied with substrate temperature due to the different batches under the same additive is shown in Fig. 4. Table 2 lists the corresponding performance parameters of OPV devices in the different batch. The performance of the new batch OPVs exhibited that PCE of devices with single additive increased with substrate temperature but demonstrated a relative lower PCE than those of the previous batch. The performance in difference between two batches was obvious. The PCE variation was much large for the devices with DIO additive. However, with increasing temperature of substrate, the PCE of devices were almost the same for different batches at the high substrate temperature of 60 °C. When the residual DIO is evaporated slowly under vacuum, $PC_{71}BM$ will be depleted in the top surface, and thus unfavorable interfacial contact will be formed [30]. Thus, PCE of the cell for single DIO additive would increase with elevated substrate temperature in our case. Also, it was found that the addition of CN into CB solution does not affect the crystallization or the molecular packing of PTB7 in the PTB7:$PC_{71}BM$ BHJ layer, but it changes the film morphology of the PTB7:$PC_{71}BM$ BHJ layers [28]. In our case with 3% CN, the film morphology might change to have moderate formation of the nano-morphology of molecules while the substrate temperature increased. Notably, the devices with DIO:CN additives still fulfilled high and stable performance in terms of V_{oc}, J_{sc}, FF and PCE compared to the lower PCE of devices with single additive. Besides, the trend in performance of devices with DIO:CN additive between different batches was almost the same, and this result implies that addition of DIO:CN additive might enhance the process stability. The cell of PTB7:$PC_{71}BM$ prepared with organic solvent additives of DIO:CN shows formation of the intermixed nano-morphology, which implies that the device performance through better intermixing between PTB7 and $PC_{71}BM$ [23]. Thus, the

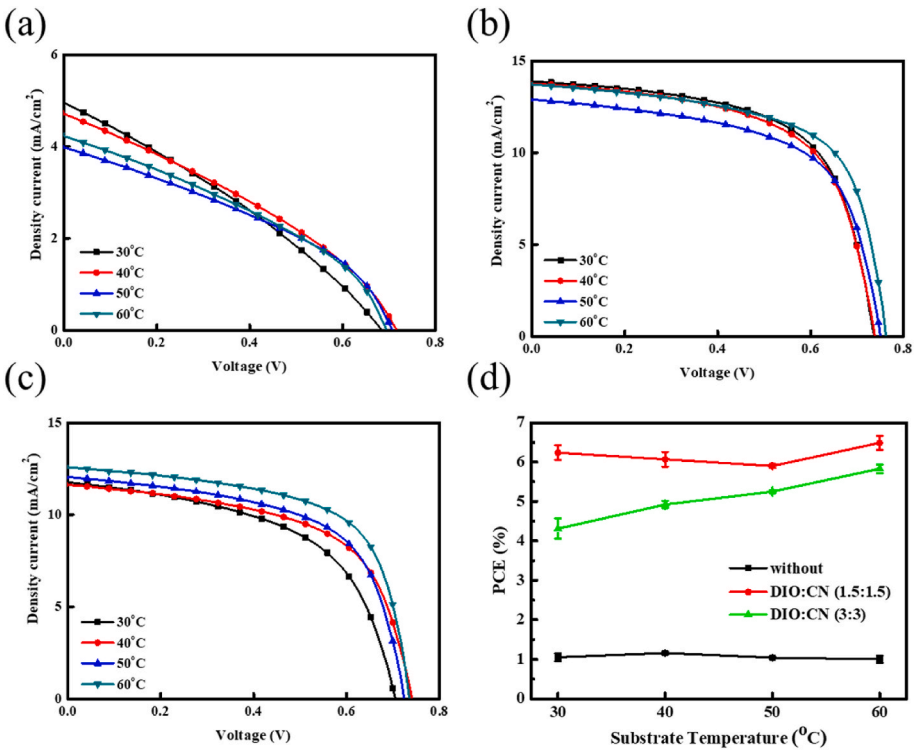

Fig. 5. (a–c) J-V curves and (d) PCE variation of S2S slot-die coated OPV devices with substrate temperature based on various additives. (a) Without additive, (b) with 1.5 vol% DIO:1.5 vol% CN, and (c) 3 vol% DIO: 3 vol% CN. The device area is 0.3 (1 × 0.3) cm^2, and the data are averaged over 20 devices. All the devices are fabricated in the same batch.

Table 3
Photovoltaic performance of the S2S slot-die coated devices corresponding to Fig. 4. The device area is 0.3 (1 × 0.3) cm^2, and the data are averaged over 20 devices. All the devices are fabricated in the same batch.

Additive(vol%)	Temperature(°C)	J_{SC}(mA/cm^2)	V_{oc}(V)	FF(%)	PCE(%)	PCE_{max}(%)
w/o	30	5.06 ± 0.08	0.67 ± 0.07	31.10 ± 1.92	1.05 ± 0.10	1.19
	40	4.65 ± 0.09	0.72 ± 0.01	34.55 ± 0.82	1.16 ± 0.04	1.21
	50	4.05 ± 0.13	0.69 ± 0.02	37.10 ± 0.68	1.04 ± 0.03	1.07
	60	4.23 ± 0.09	0.68 ± 0.02	34.65 ± 1.74	1.00 ± 0.09	1.08
DIO:CN (1.5:1.5)	30	13.86 ± 0.16	0.74 ± 0.01	61.23 ± 0.74	6.24 ± 0.19	6.38
	40	13.63 ± 0.32	0.74 ± 0.00	60.60 ± 0.18	6.07 ± 0.19	6.28
	50	12.85 ± 0.07	0.75 ± 0.00	61.17 ± 0.57	5.90 ± 0.05	5.96
	60	13.61 ± 0.21	0.76 ± 0.01	62.95 ± 0.34	6.49 ± 0.18	6.66
DIO:CN (3:3)	30	11.28 ± 0.70	0.71 ± 0.01	54.00 ± 1.13	4.31 ± 0.26	4.57
	40	11.59 ± 0.15	0.73 ± 0.01	57.93 ± 1.02	4.92 ± 0.09	5.02
	50	12.01 ± 0.08	0.73 ± 0.00	60.33 ± 0.49	5.25 ± 0.04	5.3
	60	12.66 ± 0.12	0.74 ± 0.01	62.40 ± 0.48	5.83 ± 0.11	5.95

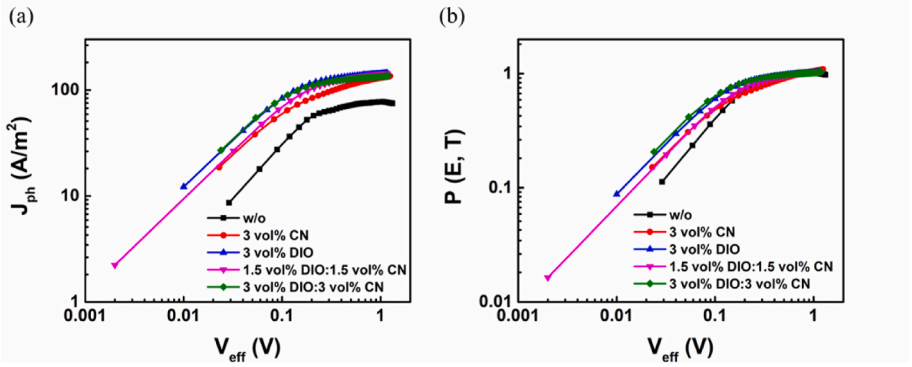

Fig. 6. Plots of (a) photocurrent density (J_{ph}) with respect to effective bias (V_{eff}) and (b) exciton dissociation probability [P (E, T)] with respect to e_{ff}ective bias (V_{eff}) for the devices with various additive systems.

Table 4
The maximum exciton generation rate (G_{max}) and exciton dissociation probability (P(E,T)) of the devices with various additives.

Additive	Gmax ($m^{-3}s^{-1}$)	P (E, T)
w/o	5.40×10^{27}	88.11
3 vol% CN	9.37×10^{27}	82.24
3 vol% DIO	9.40×10^{27}	91.95
1.5 vol% DIO:1.5 vol% CN	9.33×10^{27}	91.06
3 vol% DIO:3 vol% CN	9.13×10^{27}	89.36

temperature-independent feature of substrate temperature is demonstrated in our case. At a low substrate temperature of 30 °C, the devices with DIO:CN additive still show the same performance as the devices fabricated at 60 °C. This phenomenon can be explained by that DIO:CN additive can induce the good polymer crystallization, well-developed PCBM aggregation and suitable two-phase dispersion. The subsequent thermal annealing cannot enhance the BHJ structure.

We further increased the amount of additive in the active layer, an addition of 3 vol% DIO plus 3 vol% CN demonstrated a superior performance rather than addition of single additive in the open literature [23]. The active layer solution of PTB7:$PC_{71}BM$ without any solvent additive was prepared as the control devices, and active layer solution with addition of 3 vol% DIO plus 3 vol% CN (D3:C3) was also prepared. Fig. 5 shows the J-V curves and PCE trends of S2S slot-die coated OPV devices with substrate temperature based on the DIO:CN additives with different amount. Table 3 summarizes the device performance parameters of the corresponding OPV devices. The PCE of control devices are low at all the substrate temperatures, which is attributed to the unsuitable interpenetration network of the polymer blend and large aggregation of the $PC_{71}BM$ [34]. The PCE of devices with addition of D3:C3 additive exhibited an improved performance relative to control devices but is lower than those devices prepared with addition of DIO:CN additive. The best average performance of devices with addition of D3:C3 additive was obtained at the substrate temperature of 60 °C, with a V_{oc} of 0.74 V, a J_{sc} of 12.66 mA/cm^2, a FF of 62.40%, and a PCE of 5.83%, while the best average performance of devices with addition of DIO:CN additive in the same batch was obtained at the substrate temperature of 60 °C, with a V_{oc} of 0.76 V, a J_{sc} of 13.61 mA/cm^2, a FF of 62.95%, and a PCE of 6.49%. There was 10% of performance improvement at the substrate temperature of 60 °C, but the improvement increased with decreasing substrate temperature. The relative higher concentration of D3:C3 additives, especially at lower substrate temperature, may restrain $PC_{71}BM$ aggregation and lead to form much smaller $PC_{71}BM$ cluster, which results in discontinuity of transport path of acceptor-donor network in the active layer (i.e., over dispersion between acceptor and donor phases) and thus increasing the charge recombination rate. However, the PCE of devices with D3:C3 additive at higher substrate temperature increases, which may be attribute to partially removal of solvent additive to a proper level.

The relationship between the photocurrent density (J_{ph}) and the effective voltage (V_{eff}) is shown in Fig. 6, and the maximum exciton generation rate (G_{max}) under 1 sun irradiation, as well as the exciton dissociation probability (P(E,T)) can be calculated from these data, as listed in Table 4. In comparison to the devices without additives, the addition of solvent additives in the devices can greatly increase the exciton generation rate. Besides, the devices with mixing additive of 3% DIO and 1.5% DIO:1.5% CN exhibit better exciton dissociation probability than other systems, resulting in the increasing Jsc and FF. Moreover, we also analyzed the behavior of charge transport by using transient photovoltage (TPV) and transient photocurrent (TPC) measurement. From the results of the TPV and TPC, the carrier recombination lifetime and the carrier extraction time can be respectively obtained, further determining the influence of the additives on the charge transport behavior of our devices. The curves of TPV and TPC are shown in Fig. 7, and the fitting results are listed in Table 5. These results indicate that the solvent additives can extend the charge recombination time and reduce the charge extraction time effectively. The longest charge recombination time (24.2 μs) and the shortest charge extraction time (0.96 μs) were achieved when the devices with 1.5 vol% CN:1.5 vol % DIO, representing the best charge transport behavior.

The active area mentioned above for all the devices were only 1 × 0.3 cm^2, defined by the mask using thermal evaporated deposition. However, the film quality of slot-die coated active layers under different coating area or position is the crucial factor for scale-up process. Different recipes of using additives were evaluated based on the OPV performance of various active areas. Several devices and modules were fabricated for scale-up investigation, including devices with active area of 1 × 0.3, 1 × 1, 1 × 2, and 1 × 4 cm^2, and modules consisting of 10-cell in serial connection with cell device area of 1 × 0.2 cm^2. The total module area was actually 5 × 2 cm^2 under slot-die coated process, including the gap area between cells which contribute no effort on module performance. Fig. 8 shows the J-V curves of devices with different areas and module, and Table 6 lists the device performance parameters. The PCE loss is compared to those devices with active area of 1 × 0.3 cm^2. The OPV performance decreased gradually with increasing active area. While using single additive of DIO, the PCE losses of cells and module for different active areas of 1 × 1, 1 × 2, 1 × 4 and (1 × 0.2) × 10 cm^2 are 6.5%, −6.4%, −16.1% and −21%, respectively. With addition of single additive of DIO, the performance loss is well correlation with the scale up of total area of slot-die coated process

Table 5
Times extracted from TPV and TPC of devices based on various additives.

Additive	**Recombination time** (μs)	**Extraction time** (μs)
w/o	8.41	4.60
3 vol% CN	21.3	1.58
3 vol% DIO	22.6	0.98
1.5 vol% DIO:1.5 vol% CN	24.2	0.96
3 vol% DIO:3 vol% CN	13.1	1.72

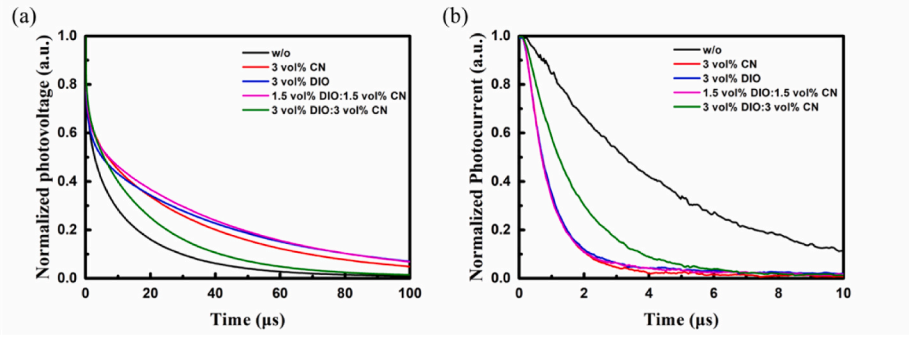

Fig. 7. (a) Transient photovoltage (TPV) and (b) transient photocurrent (TPC) measurements for the devices with various additives.

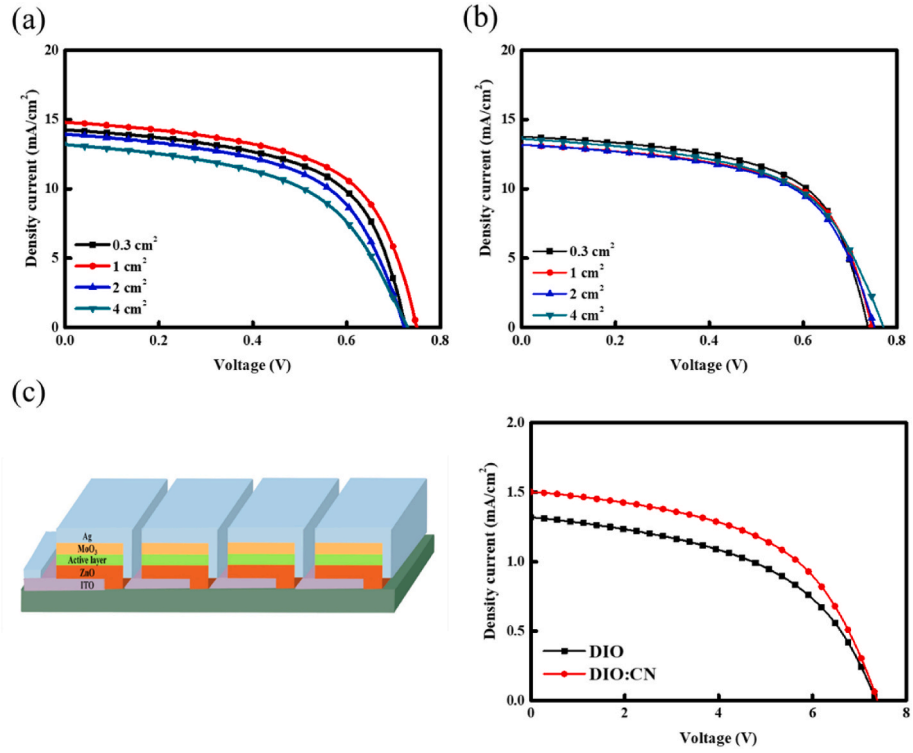

Fig. 8. J-V curves of the S2S slot-die coated (a, b) devices with different active areas and the (c) module of 10 cells in serial connection with cell area of 1 × 0.2 cm^2 based on various additives (substrate temperature is set at 50 °C). Active layer with (a) 3 vol% DIO, (b) 1.5 vol% DIO: 1.5 vol% CN.

Table 6
Photovoltaic performance of the S2S slot-die coated devices with active areas of 0.3, 1, 2, and 4 cm^2 and the module of 10 cells in serial connection with cell area of 1 × 0.2 cm^2 based on various additives (substrate temperature is set at 50 °C). The data are averaged over 20 devices. All the devices are fabricated in the same batch.

Additive	Active Area (cm^2)	J_{SC} (mA/cm^2)	V_{OC} (V)	FF (%)	PCE (%)	PCE loss (%)
DIO	1 × 0.3	13.83 ± 0.59	0.73 ± 0.01	59.88 ± 0.87	6.08 ± 0.20	—
	1 × 1	13.81 ± 0.45	0.74 ± 0.01	58.44 ± 1.75	5.94 ± 0.18	−2.3
	1 × 2	13.97 ± 0.42	0.72 ± 0.01	56.30 ± 0.41	5.69 ± 0.13	−6.4
	1 × 4	13.22 ± 0.23	0.73 ± 0.01	52.90 ± 0.56	5.10 ± 0.17	−16.1
	(1 × 0.2) × 10	1.32 ± 0.05	7.35 ± 0.11	49.50 ± 0.33	4.80 ± 0.30	−21
DIO:CN	1 × 0.3	13.63 ± 0.32	0.74 ± 0.00	60.60 ± 0.18	6.07 ± 0.19	–
	1 × 1	13.21 ± 0.16	0.75 ± 0.01	60.30 ± 0.20	5.95 ± 0.07	−2
	1 × 2	13.20 ± 0.20	0.75 ± 0.00	58.60 ± 0.10	5.82 ± 0.13	−4.2
	1 × 4	13.64 ± 0.12	0.77 ± 0.01	56.30 ± 0.22	5.91 ± 0.17	−2.7
	(1 × 0.2) × 10	1.50 ± 0.02	7.38 ± 0.09	52.30 ± 0.10	5.80 ± 0.18	−4.5

except for the device area 1 × 1 cm^2. The device of 1 × 1 cm^2, having the abnormal PCE loss, exhibits that the PCE value within the local area (~1 × 1 cm^2) has the large fluctuation in the different positions caused by the film uniformity or local BHJ structural variation. This result leads to the instability of bath-to-bath coating. The performance loss of the module is mainly due to the series connection of several cells. Performance loss of the scale-up devices and modules could be suppressed by addition of DIO:CN additive, the PCE loss for the active areas of 1 × 1, 1 × 2, 1 × 4 and (1 × 0.2) × 10 cm^2 are −2%, −4.2%, −2.7% and −4.5%, respectively. Using DIO:CN as the additive in the slot-die coated PTB7:$PC_{71}BM$ system, not only enhanced the performance for large-area devices, but also alleviated the performance loss of fabricating module with large deposition area. It might be attributed to the good BHJ structure containing the good polymer crystallinity, PCBM aggregation clusters and two-phase network formed in the entire active layer by addition of DIO:CN additive, which facilitates (1) charge carrier separation and transportation in the large-area film and (2) film uniformity.

According to our previous research [31], the BHJ nano-morphology is strongly influenced by the drying process to evaporate the solvent for forming the solid-state film (i.e., early polymer crystallization) during the R2R slot-die coating process. As we mentioned above, the film prepared with DIO:CN additives can be tailored to have appropriate nanostructure, including good polymer crystallization, PCBM aggregation and thus suitable phase separation. The surface roughness of the slot-die coated active layers represents the interfacial contact between active layer and electron transport layer. Moreover, the low surface roughness of active layer also implies an improved interfacial contact between the active layer and MoO_3/Ag anode. In comparison to active layer with single additive, the active layer with DIO:CN additive exhibits low surface roughness (7.9 nm) even at low processing temperature of 30 °C, resulting in better interfacial contact between active layer and electrode. The stability of the devices with various additives is shown in Fig. 9. We put the devices with various additives in glove box and dry box (relative humidity ~ 40%) for 250 h. Compared with other devices, the devices with 1.5%DIO:1.5%CN exhibit higher stability.

4. Conclusions

The film uniformity and PCE stability between batches of slot-die coated PTB7:$PC_{71}BM$ active layer were evaluated by controlling solvent additives as recipe. The best performance of OPVs is achieved by addition of DIO:CN (DIO 1.5 vol% and CN 1.5 vol%) additive. OPV performance based on single additive, including DIO or CN, is of large

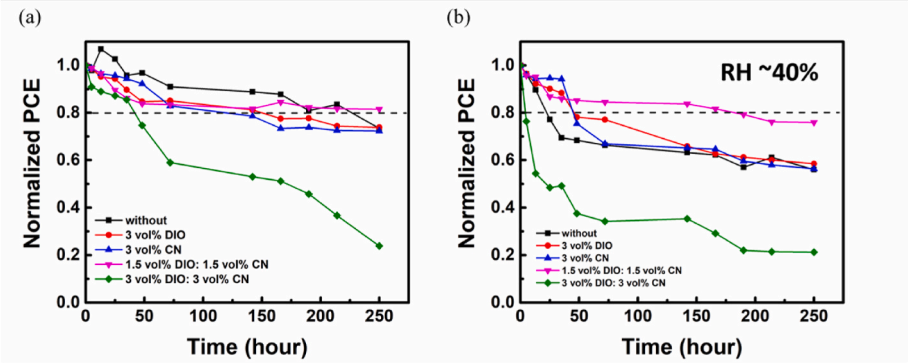

Fig. 9. (a) Normalized PCE variation of device with different additives (a) in the glove box and (b) the dry box (relative humidity ~ 40%).

fluctuation (or called unstable) in different batches and in different local areas of the same coating batch. For solving these problems, addition of DIO:CN additive in the active layer can yield the relatively high performance. Moreover, the substrate temperature-independent feature of DIO:CN additive facilitates the wet coating of the active layer with a broad processing window, lowering the threshold limitation for mass production. Besides, the OPVs prepared by DIO:CN additive demonstrates equal performance at the substrate temperatures ranging from 30 °C to 60 °C, indicating that the less energy input shortens energy payback time. Over addition, DIO 3 vol% and CN 3 vol%, will induce a detrimental effect. Elevating substrate temperature is needed to eliminate the negative effect due to excess additives in the active layer for achieving good performance. Superior performance in the large area devices and modules by employing DIO:CN additive paves a way for the realization of scalable commercialization.

CRediT authorship contribution statement

Hou-Chin Cha: Methodology, Investigation. **Yu-Ching Huang:** Conceptualization, Project administration, Funding acquisition, Writing – original draft, Supervision, Writing – review & editing. **Chia-Feng Li:** Visualization, Investigation. **Cheng-Si Tsao:** Supervision, Writing – review & editing.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

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